## What Is Claimed Is:

1	1. A method for generating code to perform anticipatory prefetchin	ıσ
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	for data references, comprising:	
3	receiving code to be executed on a computer system;	
4	analyzing the code to identify data references to be prefetched; and	
5	inserting prefetch instructions into the code in advance of the identified	
6	data references, wherein inserting the prefetch instructions involves,	
7	attempting to calculate a stride value for a given data	
8	reference within a loop,	
9	if the stride value cannot be calculated, setting the stride	
0	value to a default stride value, and	
1	inserting a prefetch instruction to prefetch the given data reference for a	
2	subsequent loop iteration based on the stride value.	
1	2. The method of claim 1, further comprising allowing a system use	er
2	to specify the default stride value.	
1	3. The method of claim 1, wherein calculating the stride value	
2	involves:	
3	identifying an induction variable for the stride value;	
4	identifying a stride function for the stride value; and	
5	calculating the stride value based upon the stride function and the	
6	induction variable.	
1	4. The method of claim 1, wherein inserting the prefetch instruction	1
2	based on the stride value involves:	•
3	calculating a prefetch cover distance by dividing a cache line size by the	
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4	stride value;	
5	calculating a prefetch ahead distance as a function of a prefetch latency,	
6	the prefetch cover distance and an execution time of a loop; and	
7	calculating a prefetch address by multiplying the stride value by the	
8	prefetch cover distance and the prefetch ahead distance and adding the result to an	
9	address accessed by the given data reference.	
1	5. The method of claim 1, wherein analyzing the code involves:	
2	identifying loop bodies within the code; and	
3	identifying data references to be prefetched from within the loop bodies.	
1	6. The method of claim 5, wherein analyzing the code to identify data	
2 references to be prefetched involves examining a pattern of data references		
3	multiple loop iterations.	
1	7. The method of claim 1, wherein analyzing the code involves	
2	analyzing the code within a compiler.	
1	8. A computer-readable storage medium storing instructions that	
2	when executed by a computer cause the computer to perform a method for	
3	generating code to perform anticipatory prefetching for data references, the	
4	method comprising:	
5	receiving code to be executed on a computer system;	
6	analyzing the code to identify data references to be prefetched; and	
7	inserting prefetch instructions into the code in advance of the identified	
8	data references, wherein inserting the prefetch instructions involves,	
9	attempting to calculate a stride value for a given data	
10	reference within a loop,	
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11	if the stride value cannot be calculated, setting the stride	
12	value to a default stride value, and	
13	inserting a prefetch instruction to prefetch the given data	
14	reference for a subsequent loop iteration based on the stride value.	
1	9. The computer-readable storage medium of claim 8, wherein the	
2	method further comprises allowing a system user to specify the default stride	
3	value.	
1	10. The computer-readable storage medium of claim 8, wherein	
2	calculating the stride value involves:	
3	identifying an induction variable for the stride value;	
4	identifying a stride function for the stride value; and	
5	calculating the stride value based upon the stride function and the	
6	induction variable.	
1	11. The computer-readable storage medium of claim 8, wherein	
2	inserting the prefetch instruction based on the stride value involves:	
3	calculating a prefetch cover distance by dividing a cache line size by the	
4	stride value;	
5	calculating a prefetch ahead distance as a function of a prefetch latency,	
6	the prefetch cover distance and an execution time of a loop; and	
7	calculating a prefetch address by multiplying the stride value by the	
8	prefetch cover distance and the prefetch ahead distance and adding the result to an	
9	address accessed by the given data reference.	
1	12. The computer-readable storage medium of claim 8, wherein	
2	analyzing the code involves analyzing the code within a compiler.	
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i	An apparatus that generates code to perform anticipatory		
2	prefetching for data references, comprising:		
3	a receiving mechanism that is configured to receive code to be executed		
4	on a computer system;		
5	an analysis mechanism that is configured to analyze the code to identify		
6	data references to be prefetched; and		
7	an insertion mechanism that is configured to insert prefetch instructions		
8	into the code in advance of the identified data references;		
9	wherein the insertion mechanism is configured to,		
0	attempt to calculate a stride value for a given data reference		
1	within a loop,		
2	set the stride value to a default stride value if the stride		
3	value cannot be calculated, and to		
4	insert a prefetch instruction to prefetch the given data		
5	reference for a subsequent loop iteration based on the stride value.		
1	14. The apparatus of claim 13, further comprising a configuration		
2	mechanism that is configured to receive the default stride value from a system		
3	user.		
1	15. The apparatus of claim 13, wherein while calculating the stride		
2	value, the insertion mechanism is configured to:		
3	identify an induction variable for the stride value;		
4	identify a stride function for the stride value; and to		
5	calculate the stride value based upon the stride function and the induction		
6	variable.		

1	16. The apparatus of claim 13, wherein the insertion mechanism is	
2	configured to:	
3	calculate a prefetch cover distance by dividing a cache line size by the	
4	stride value;	
5	calculate a prefetch ahead distance as a function of a prefetch latency, the	
6	prefetch cover distance and an execution time of a loop; and to	
7	calculate a prefetch address by multiplying the stride value by the prefetch	
8	cover distance and the prefetch ahead distance and adding the result to an address	
9	accessed by the given data reference.	
1	17. The apparatus of claim 13, wherein the apparatus resides within a	
2	compiler.	
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2	18. A method for generating code to perform anticipatory prefetching for data references, comprising:	
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	receiving code to be executed on a computer system;	
4	analyzing the code to identify data references to be prefetched; and	
5	inserting prefetch instructions into the code in advance of the identified	
6	data references so that multiple prefetch instructions are issued for a given data	
7	reference;	
8	whereby the given data reference is prefetched even if the computer	
9	system drops a prefetch instruction for the given data reference.	
1	19. The method of claim 18, wherein inserting prefetch instructions	
2	involves ensuring that the multiple prefetch instructions for the given data	
3	reference are issued at different times, so that a single event is unlikely to cause	
4	all of the multiple prefetch instructions for the given data reference to be dropped	
5	by the computer system.	

1	20. The method of claim 18, wherein inserting prefetch instructions	
2	involves issuing each of the multiple prefetch instructions for the given data	
3	reference in a different loop iteration.	
1	21. The method of claim 18, wherein analyzing the code involves:	
2	identifying loop bodies within the code; and	
3	identifying data references to be prefetched from within the loop bodies	
1	22. The method of claim 21, wherein analyzing the code to identify	
2	data references to be prefetched involves examining a pattern of data references	
3	over multiple loop iterations.	
1	23. The method of claim 18, wherein analyzing the code involves	
2	analyzing the code within a compiler.	
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1	24. A computer-readable storage medium storing instructions that	
2	when executed by a computer system cause the computer system to perform a	
3	method for generating code to perform anticipatory prefetching for data	
4	references, the method comprising:	
5	receiving code to be executed on the computer system;	
6	analyzing the code to identify data references to be prefetched; and	
7	inserting prefetch instructions into the code in advance of the identified	
8	data references so that multiple prefetch instructions are issued for a given data	
9	reference;	
10	whereby the given data reference is prefetched even if the computer	
11	system drops a prefetch instruction for the given data reference.	

1	25. The computer-readable storage medium of claim 24, wherein
2	inserting prefetch instructions involves ensuring that the multiple prefetch
3	instructions for the given data reference are issued at different times, so that a
4	single event is unlikely to cause all of the multiple prefetch instructions for the
5	given data reference to be dropped by the computer system.
1	26. The computer-readable storage medium of claim 24, wherein
2	inserting prefetch instructions involves issuing each of the multiple prefetch
3	instructions for the given data reference in a different loop iteration.
1	27. The computer-readable storage medium of claim 24, wherein
2	analyzing the code involves analyzing the code within a compiler.
1	28. An apparatus that generates code to perform anticipatory
2	prefetching for data references, comprising:
3	a receiving mechanism that is configured to receive code to be executed
4	on a computer system;
5	an analysis mechanism that is configured to analyze the code to identify
6	data references to be prefetched; and
7	an insertion mechanism that is configured to insert prefetch instructions
8	into the code in advance of the identified data references so that multiple prefetch
9	instructions are issued for a given data reference;
10	whereby the given data reference is prefetched even if the computer
11	system drops a prefetch instruction for the given data reference.

configured to ensure that the multiple prefetch instructions for the given data

reference are issued at different times, so that a single event is unlikely to cause

The apparatus of claim 28, wherein the insertion mechanism is

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4	all of the mu	ltiple prefetch instructions for the given data reference to be dropped
5	by the compu	iter system.
1	30.	The apparatus of claim 28, wherein the insertion mechanism is
2	configured to	issue each of the multiple prefetch instructions for the given data
3	reference in a	a different loop iteration.
1	31.	The apparatus of claim 28, wherein the apparatus resides within a
2	compiler.	
1	32.	A method for generating code to perform anticipatory prefetching
2	for data references, comprising:	
3	receiv	ving code to be executed on a computer system;
4	analy	zing the code to identify data references to be prefetched; and
5	insert	ing prefetch instructions into the code in advance of the identified
6	data referenc	es;
7	where	ein inserting the prefetch instructions involves,
8		identifying a location in the code where a prefetch address
9		for a given prefetch instruction is calculated, and
10		inserting the given prefetch instruction as far ahead of a
11		corresponding data reference operation as possible, but not before
12		the location where the prefetch address is calculated.
1	33.	The method of claim 32, wherein inserting the given prefetch
2	instruction ca	an involve inserting the given prefetch instruction into a preceding

block in the code.

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1	34. The method of claim 33, wherein inserting the given prefetch	
2	instruction involves:	
3	tracing execution of the code to produce an execution trace;	
4	using the execution trace to identify a preceding block in which the	
5	prefetch address is calculated; and	
6	inserting the given prefetch instruction into the preceding block after the	
7	location where the prefetch address is calculated.	
1	35. The method of claim 32, wherein analyzing the code involves:	
2	identifying loop bodies within the code; and	
3	identifying data references to be prefetched from within the loop bodies.	
1	36. The method of claim 35, wherein analyzing the code to identify	
2	data references to be prefetched involves examining a pattern of data reference	
3	over multiple loop iterations.	
1	37. The method of claim 32, wherein analyzing the code involves	
2	analyzing the code within a compiler.	
1	38. A computer-readable storage medium storing instructions that	
2	when executed by a computer cause the computer to perform a method for	
3	generating code to perform anticipatory prefetching for data references, the	
4	method comprising:	
5	receiving code to be executed on a computer system;	
6	analyzing the code to identify data references to be prefetched; and	
7	inserting prefetch instructions into the code in advance of the identified	
3	data references;	
)	wherein inserting the prefetch instructions involves,	
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1	identifying a location in the code where a prefetch address
2	for a given prefetch instruction is calculated, and
3	inserting the given prefetch instruction as far ahead of a
4	corresponding data reference operation as possible, but not before
5	the location where the prefetch address is calculated.
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1	39. The computer-readable storage medium of claim 38, wherein
2	inserting the given prefetch instruction can involve inserting the given prefetch
3	instruction into a preceding block in the code.
1	40. The computer-readable storage medium of claim 38, wherein
2	inserting the given prefetch instruction involves:
3	tracing execution of the code to produce an execution trace;
4	using the execution trace to identify a preceding block in which the
5	prefetch address is calculated; and
6	inserting the given prefetch instruction into the preceding block after the
7	location where the prefetch address is calculated.
1	41. The computer-readable storage medium of claim 38, wherein
2	analyzing the code involves analyzing the code within a compiler.
1	42. An apparatus that generates code to perform anticipatory
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3	prefetching for data references, comprising:
	a receiving mechanism that is configured to receive code to be executed
4 ~	on a computer system;
5	an analysis mechanism that is configured to analyze the code to identify
6	data references to be prefetched; and

7	an in	sertion mechanism that is configured to insert prefetch instructions
8	into the code	e in advance of the identified data references;
9	wher	ein the insertion mechanism is configured to,
10		identify a location in the code where a prefetch address for
11		a given prefetch instruction is calculated, and to
12		insert the given prefetch instruction as far ahead of a
13		corresponding data reference operation as possible, but not before
14		the location where the prefetch address is calculated.
1	43.	The apparatus of claim 42, wherein the insertion mechanism is
2	configured to insert the given prefetch instruction into a preceding block in the	
3	code.	
1	44.	The apparatus of claim 43, wherein the insertion mechanism is
2	configured to	
3	trace execution of the code to produce an execution trace;	
4	use the execution trace to identify a preceding block in which the prefeto	
5	address is calculated; and to	
6	insert the given prefetch instruction into the preceding block after the	
7	location when	re the prefetch address is calculated.
1	45.	The apparatus of claim 42, wherein the apparatus resides within a
2	compiler.	